Low Power High Gain CMOS LNA for WLAN and ISM Band Applications

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Abstract—A 1.8V, 2.4 GHz CMOS low noise amplifier (LNA) is proposed to be used in front end receiver of Wireless LAN (WLAN) and Industrial Scientific and Medicine (ISM) band. The circuit is simulated in tsmc 180nm V 3.2. The optimization for the width of the CMOS is done taking into consideration parameters viz. noise figure (NF), Power consumption, gain, stability and linearity. The matching of input capacitance and that of output capacitance for a particular width of the CMOS is used to obtain tradeoffs between the design parameters. The LNA power gain($S_{21}$) is 24.60 dB, noise figure is 1.26dB, reverse isolation is -35.3 dB, input return loss ($S_{11}$) is -10.41 dB, output return loss ($S_{22}$) is -11.28 dB and the power consumption is 2.26 mW from a single 1.8 V power supply. The main features of proposed design of LNA are low noise figure and low power consumption without affecting the gain in the range of consideration.

Keywords—CMOS, low noise amplifier (LNA), input matching, Noise Figure, Power gain, Stability, Wireless LAN

I. INTRODUCTION

There is rapid development in the field of wireless communication which makes demand for low-cost, high-performance and high-integration technology. System on a chip (SOC) implementation is also one of the key areas of development these days. The wide acceptance of wireless products is due to the advancement of device technology, and continuous improvement in the semiconductor processes[1]. RF integrated circuits (RFICs) are implemented in GaAs process technologies because of their relatively high unity gain frequency $f_T$. The recent improvements in speed of the standard CMOS process had made the unity gain frequency $f_T$ of CMOS device comparable to that of the GaAs process. The other advantages of the CMOS process are low cost and high integration with baseband digital circuits. Therefore the CMOS technology provides a good solution for SOC integration. These advancements in digital CMOS technology have made possible the implementation of the integrated circuits operating at microwave frequency bands. The CMOS technology platform is today’s mainstream in analog mixed signal and RFIC implementation.

To handle the market demands, emergence of new wireless communication systems is there. Being pushed by market demands, various wireless communication systems are emerging. Wireless local area networks (WLANs) have been introduced in ISM and UNII bands for indoor wireless access. IEEE 802.16a Wireless Metropolitan Area Networks (WMANs) standard [2] for urban area coverage wireless access as the “last mile” solution. IEEE 802.16a system addresses frequencies from 2 to 11GHz, including licensed and un-licensed bands while the dominant bands[2] are licensed bands of 2.3 GHz (WCS), 2.5 to 2.7 GHz (MMDS), 3.5 to 3.7 GHz (ETSI), and unlicensed bands of 2.4 GHz (ISM) and 5.8 GHz (U-NII) where WLANs operates as well.

Wireless receivers need to detect and amplify incoming low power signals without adding much noise. The most common solution is the use of low noise amplifier (LNA) as the first stage. LNA is one of the important and most challenging block in the front end receiver. The role of LNA is to provide a decent low noise amplification of the signal to the next stage in the circuit. The design methods for CMOS LNAs are very limited[3]. As most of the advancements is done in BJT stage with architecture. A CMOS LNA design present considerable challenge done to it simultaneous requirement for high gain, low noise figure, impedance matching and circuit stability in corresponding frequency bands with reduction in power consumption, leading to increased battery life.

The appropriate LNA design is crucial in today’s communication solutions due to complexity of the signals. Additional design considerations need to be addressed during design procedure. In this paper section 2 discusses the architecture selection in accordance with our specifications viz. noise figure, power consumption and impedance matching. Section 3 covers the LNA design.
Section 4 covers the simulation results and Section 5 gives the conclusion.

II. LNA ARCHITECTURE

The various topologies for LNA have the disadvantages of their own. Resistive terminations have deleterious effect on the amplifier’s noise figure. The common gate approach is also not being considered because of its high noise figure. The common gate approach is also not being considered because of its high noise figure. The shunt series feedback topology has considerable gain; along with noise figure same as that of other topologies. The shunt series feed back topology is having broadband response pertaining to which it is having higher power dissipation as compared to other topologies. We have used the inductive source degeneration architecture (Fig. 1) for our design as it is having lower power dissipation because of its narrowband approach. The other important advantage of this method is that there is a good control over the real part of the impedance through the choice of inductance chosen by the designer. Inductive source or emitter degeneration is being employed in this technique. By using this technique it is possible to achieve the best noise performance for any architecture we are using depending upon the requirement[4].

![Fig. 1. Inductively Degenerated CMOS LNA](image)

The input impedance has the following form [5]

$$Z_i = j\omega (L_s + L_g) - \frac{1}{\omega C_{gs}} + \alpha l L_s$$

(1)

Where $L_g$ is the gate inductor, $L_s$ is the source inductor, $C_{gs}$ is the gate to source capacitor, $\omega$ $T$ is the transition frequency. Cascode topology is being extensively used for most of CMOS LNA designs as cascode amplifiers have the benefit of low power consumption along with minimum noise figure simultaneously and it also provides good isolation between input and output stages of the LNA. The topology shown in Fig. 2 utilizes two MOS transistors connected from source to the drain of other MOS. Normally the bias voltage of the transistors is applied from the gate of the top transistor. The main concerns for designing amplifiers are stability of the amplifier. The cascoding of transistor M2 reduces the interaction of the tuned output with the tuned input and also reduce the drain gate capacitance of M1.

![Fig. 2. Designed and Simulated LNA](image)

The total node capacitance at drain of M2 resonates with inductance $L_d$ both to increase the gain at the centre frequency and side by side it will provide an additional level of highly desirable band pass filtering. The isolation of Miller capacitance of first transistor to that of second transistor is obtained by cascading. By using this topology there is considerable reduction in power consumption and increase in reverse isolation, $S_{12}[6]$. The noise figure derived from the noise model is given by equation (2) and can be calculated from the equation[11]. The correlation coefficient $c$ for the 0.18µm technology is $c \cong -j0.55$ when MOS is working in inversion mode [12].

$$F = 1 + \frac{R}{R_F} \left[ \frac{\delta C}{5\gamma} + \frac{\delta C}{5\gamma} + \frac{\delta C}{5\gamma} + \frac{\delta C}{5\gamma} + \frac{\delta C}{5\gamma} + \frac{\delta C}{5\gamma} \right]$$

(2)

III. LNA DESIGN

The proposed Single ended degenerated LNA is shown in Fig. 2 [4]. The transistor M1 forms the input of the LNA; M2 for the output of the LNA and M3 along with M1 is used for biasing. A current mirror is formed by M1 and M3, thus a stable input is being assured to the M3 thus it makes sure that transistors always remain in saturation region which is required for the desired results of LNA. The size of M1 is kept same as that of M2 so as to reduce and suppress the noise magnitude of M2 and the Miller effect of M1, arising because of $C_{gd}[4].$ The width of M3 is small fraction of M1 so that it can be utilized as current mirror. In this design $W_1 = 20W_3$, where $W_1$ = width of transistor M1 and $W_3$ = width of transistor M3.
The capacitors $C_{in}$ and $C_{load}$ DC blocking capacitors play very important role in input and output matching of LNA. The load capacitor $C_{load}$ is tuned to manage the trade off between gain, output matching and power dissipation of LNA. The input and output impedance is matched at 50Ω. The width of the input transistor is given by equation (3)[5]

$$W_t = W_{opt} = \frac{1}{3\omega C_{ox} R_s}$$

where $C_{ox}$ is the oxide capacitance, $\omega$ is the operating frequency; $L$ is the effective length of the transistor as per the technology and $R_s$ is the source resistance which is 50Ω in this design. The value of $L_s$, $L_g$ can be found using equation (1) by matching the input impedance. Also the value of $L_d$ can be obtained by matching the output transistor M3.

**IV. SIMULATION RESULTS OF LNA**

The LNA is designed for 0.18µm CMOS technology. EldoRF from Mentor Graphics software is used for circuit design and simulation. Once the width of the device is fixed, then the trade offs between group of two variables are made in this design, by adjusting the input and output capacitances $C_{in}$ and $C_{load}$ respectively. The designed LNA is being driven using 1.8 V supply voltage and consumes 2.26 mW. The simulation results for CMOS LNA are shown in Fig. 3 to Fig. 6. Fig. 3 shows a plot of the Noise figure versus frequency for the LNA at 1.8V supply, the LNA achieves Noise Figure of 1.26 dB at 2.4 GHz. The LNA has a power gain of 24.60 dB at 2.4 GHz as shown in Fig. 4. The voltage gain of LNA is 27.95 dB at 2.4 GHz as shown in Fig. 5. The Fig. 6 shows the input and output return losses ($S_{11}$ & $S_{22}$), input return loss ($S_{11}$) of –10.41 dB and output return loss ($S_{22}$) of -11.24 dB are obtained at 2.4 GHz. Fig. 7 shows the bandwidth of LNA which is 102.10 MHz. The linearity as measured as IIP3 is -4.32 while the sensitivity of the LNA is tested at -85 dBm.

Table I shows a summary of the proposed 2.4 GHz CMOS LNA characteristics.

**TABLE I**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>tsmc 0.18µm</td>
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</tbody>
</table>
The performance of LNA represents low power, high gain and low noise and a comparison with other similar LNA is shown in Table II.

**TABLE II**
Performance and Comparison with other LNA’s

<table>
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<tr>
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</thead>
<tbody>
<tr>
<td>Center Frequency (GHz)</td>
<td>2.4</td>
<td>2.4</td>
<td>2.4</td>
<td>2.4</td>
<td>2.4</td>
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<tr>
<td>Input Return Loss (S11)</td>
<td>-10.41</td>
<td>-10.62</td>
<td>-14</td>
<td>-10.1</td>
<td></td>
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<tr>
<td>Reverse Isolation(S12)</td>
<td>-35.13</td>
<td>-27.3</td>
<td>-15</td>
<td>-10.1</td>
<td></td>
</tr>
<tr>
<td>Output Return Loss (S21)</td>
<td>-11.28</td>
<td>-9.6</td>
<td>-10.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NF</td>
<td>1.26</td>
<td>2.0</td>
<td>2.2</td>
<td>2.7</td>
<td>2.7</td>
</tr>
<tr>
<td>IP3</td>
<td>-4.32</td>
<td>-10.6</td>
<td>-1.5</td>
<td>3.3</td>
<td>-4</td>
</tr>
<tr>
<td>PDC (mW)</td>
<td>2.26</td>
<td>4.45</td>
<td>2.7</td>
<td>1.7</td>
<td>11.7</td>
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<tr>
<td>Supply Voltage</td>
<td>1.8</td>
<td>1.5</td>
<td>1.8</td>
<td>1.8</td>
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</tr>
<tr>
<td>Technology used</td>
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<td>0.18 μm CMOS</td>
<td>0.18 μm CMOS</td>
<td>0.18 μm CMOS</td>
<td>0.18 μm CMOS</td>
</tr>
<tr>
<td>Voltage gain (dB)</td>
<td>27.95</td>
<td>31.6</td>
<td>31.6</td>
<td>31.6</td>
<td>31.6</td>
</tr>
</tbody>
</table>

V. CONCLUSION

This paper presents a design of low noise low power CMOS LNA for WLAN and ISM band. The LNA has been designed in TSMC 0.18μm CMOS technology. The trade-offs among noise figure, gain and power consumption is achieved in this design. The LNA achieves a noise figure of 1.26 dB with input return loss of -10.41 dB and output return loss of -11.42 dB. The small signal gain S21 is 24.60 dB. The voltage gain for the LNA is 27.95. The bandwidth obtained for the design is 75.983 MHz is appreciable and it can also be used for Bluetooth applications. The power consumption is 2.26 mW is one of the best features of the design along with reverse isolation of 37.1 dB at 2.4 GHz.

REFERENCES


