High Voltage Piezoelectric Generators Using CMOS Integrated Circuit

Yuvraj Singh Ranawat  
Scholar M.Tech  
Mewar University

Girish K. Dalal  
Assistant Professor  
Mewar University

Munendra Kumar  
Assistant Professor  
Mewar University

Ashutosh Dwivedi  
Assistant Professor  
MIT Moradabad

INTRODUCTION

Piezoelectric generators (PGs) are widely used to harvest ambient vibration, i.e., convert vibration energy into electrical energy which can be used to supply low-power electronics like wireless sensor nodes [1]. Since vibration appears discontinuously, the converted energy has to be stored on a large storage capacitor. A non-linear interface circuit connected between the PG and the storage capacitor can increase the power output of the PG [2]. In order to not cancel out this benefit, the power consumption of the interface has to be orders of magnitude smaller than the transferred power. The interface circuit uses a coil as temporary energy storage, and several switches control the current flow between the PG, the coil, and the storage capacitor.

The usage of CMOS technology reduces the power consumption compared to discrete electronics, but the maximum allowed voltages are lower. The integrated interface circuit (IIC) presented in [3] works efficiently in a very limited range of PG voltage amplitudes (1.2 V–2.4 V). In addition, an external power supply is necessary to drive the MOSFET switches. In [4], both drawbacks are resolved: The presented IIC operates completely energy autonomously and is able to process PG voltage amplitudes up to 7 V. Since the voltage amplitude of PGs with a reasonable output power of some mill watts can reach some 10 V [5], the goal of this work is to develop a low-power IIC operable within this voltage range. The IIC presented in this paper is a further development of [4]. By usage of high voltage MOSFETs, PG voltages up to 18 V are allowed. The usage of these special devices requires a slightly higher supply voltage of 2.5 V for acceptable on-resistance. Moreover, the energy loss of the IIC caused by the parasitic resistances of the rectifier, the switches, and the coil is reduced by implementation of an improved switching technique [6]. Simulations show that the efficiency is thus increased by about 8%.

SWITCHING TECHNIQUE CONSIDERATIONS

Fig. 1 shows the position of the switches S1, S213, S223 and S3 within the IIC. The term "switching technique" describes the method of turning these switches on and off in order to perform the transfer process. In the following, the formerly used switching technique ST13 and the improved switching technique ST23 [6] are described (see also Fig. 2).

At the beginning of a PG cycle, all switches are off. Since the PG is unloaded due to the open circuit configuration, the rectified PG voltage VRec rises freely (phase A). When VRec has reached a maximum voltage VRce0, the transfer process is initiated starting with phase B. The switch configuration in this phase depends on the ratio x = VRec0/V Stor where V Stor is the voltage of the storage capacitor. If x < 2, S1 is turned on so that the energy stored on the PG is transferred completely from

ABSTRACT

This work presents a CMOS integrated interface circuit (IIC) enabling highly efficient energy transfer from piezoelectric generators (PGs) to a storage element, e.g., a large capacitor. Due to the low power consumption of 4.7 μW assuming a supply voltage of 2.5 V, the IIC can be supplied totally by the storage capacitor. The storage capacitor can be passively charged via a bypassing circuit if its voltage is not sufficient to supply the control circuit. PG voltage amplitudes of up to 18 V are tolerated by using special high voltage transistors. Using an improved switching technique, simulations suggest an efficiency gain of about 8% compared to a formerly-used switching technique, resulting in efficiency between 80% and 90% for PG voltage amplitudes higher than 6 V.

Key Words: Piezoelectric Energy Harvesting, CMOS Integrated Interface Circuit, Nonlinear Power Extraction
the PG capacitor into the coil. In case of $x > 2$, the improved switching technique ST23 is enabled, which means that S223 is turned on. As a result, the energy is carried into the coil and the storage capacitor at the same time. If ST23 would be enabled while $x < 2$, energy would remain at the end of phase B, making this technique inefficient.

After $V_{Rec}$ has dropped to 0 V, i.e. the total energy has been transferred from the PG to the coil, phase C starts. During this phase which is equal for both ST13 and ST23, S213/S223 and S3 are on, resulting in an energy transfer from the coil into the storage capacitor. After this phase, all switches are turned off and a new cycle starts.

In order to create a switching technique functional for all $x > 0$, ST13 for $x < 2$ and ST23 for $x > 2$ can be combined, resulting in a new switching technique named ST1323.

CIRCUIT DESIGN

Fig. 1 shows the block diagram of the energy harvesting system. The PG, the coil $L$ and the storage capacitor are connected to the IIC externally. In the following, the parts of the IIC are described in detail.

Switches

In order to withstand voltages up to 18 V, special high voltage transistors are used. The switches S1 and S3 are n-channel MOSFETs with a $W/L$ ratio of $30 \text{ mm}/3.5 \mu\text{m}$, the switches S213 and S223 are p-channel MOSFETs with a $W/L$ ratio of $30 \text{ mm}/2.5 \mu\text{m}$. The bulk regulation is necessary in order to prevent current flow through bulk diodes causing latch-ups.

The high level of $V_{GateS1}$ and $V_{GateS3}$ is simply $V_{Stor}$, but the high level of $V_{GateS213}$ and $V_{GateS223}$ has to be defined by $\max(V_{Rec},V_{Stor})$ in order to keep the according PMOS transistors closed if $V_{Rec}>V_{Stor}$.

Rectifier

An active rectifier using MOSFETs driven by an ultra-low-power-comparator and a passive rectifier using cross-coupled MOSFETs are connected in parallel [3]. The active rectifier works highly efficient only if $V_{Stor}>1.3$ V since the ultra-low-power-comparator is supplied by the storage capacitor. The passive rectifier ensures low-efficient rectification on startup when $V_{Stor}$ is too low.

Bypass and power-on-reset

The switch control circuit is supplied by the storage capacitor. $V_{Stor}$ needs to be larger than about 1.3 V in order to ensure proper operation. If $V_{Stor}$ is too low on startup, the supply rail of the switch control circuit is disconnected from the storage capacitor by a power-on-reset circuit (POR). In this case, the storage capacitor is charged passively via the bypass. This part mainly consists of a diode-connected PMOS which can be enabled and disabled.

Switch control circuit

Fig. 3 shows the switch control circuit generating the gate signals for the MOSFET switches. The timing mainly depends on $V_{Rec}$. Since this represents an event-driven timing, static RS latches are used to generate the switch control signals.
The peak detector [4] and the zero crossing detector [3] generate a short pulse when \( V_{\text{Rec}} \) has crossed a peak and a \(-100 \text{ mV} \) threshold, respectively. The reverse current barrier [4] prevents goldcap discharge after completion of the transfer process. A fast comparator Comp RCB turns the switches S213 and S223 off when their voltage drop gets negative indicating a reverse current. By comparing \( V_{\text{DD}} = V_{\text{Stor}} \) and \( V_{\text{Rec}}/2 = V_{\text{Rec}0}/2 \) using the comparator CompST, the switchover between ST13 and ST23 is performed. If \( V_{\text{Rec}0}/2 < V_{\text{Stor}} \) which is equivalent to \( x < 2 \), ST13 is enabled by pulling the signal ST high. Thus, switch S223 (PMOS) is disabled due to \( \text{Gate}_{\text{S223}} = \text{high} \) and switches S1 and S213 are enabled. If \( x > 2 \), ST is low and thus S1 and S213 are disabled whereas S223 is enabled. In order to minimize the power consumption, the zero crossing detector and CompRCB are activated only during phase B and phase C, respectively. The peak detector has to be enabled permanently since it initiates the transfer process. Since the decision of the appropriate switching technique has to be made exactly in the moment when \( V_{\text{Rec}} \) peaks, CompST has to be turned on permanently, too.

**SIMULATION RESULTS AND DISCUSSION**

The complete circuit has been designed in a 0.35 µm CMOS process and simulated using Cadence Spectre. An equivalent circuit consisting of an AC current source and internal impedance models the PG (Fig. 1). The current source emulates a sinusoidal excitation; the parallel connection \( R_{P} \) - \( C_{p} \) represents the internal capacitor including ohmic losses. The used electrical parameters are listed in Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \omega/2\pi )</td>
<td>250 Hz</td>
</tr>
<tr>
<td>( C_{s} )</td>
<td>12 nF</td>
</tr>
<tr>
<td>( R_{R} )</td>
<td>36 kΩ</td>
</tr>
<tr>
<td>( L )</td>
<td>100 µH</td>
</tr>
<tr>
<td>( R_{\text{Coil}} )</td>
<td>1 Ω</td>
</tr>
<tr>
<td>( V_{\text{Stor}} )</td>
<td>2.5 V</td>
</tr>
</tbody>
</table>

The initial condition \( V_{\text{Stor}} = 2.5 \text{ V} \) emulates a sufficiently charged storage capacitor. This voltage is a reasonable tradeoff between the resulting on-resistance of the MOSFET switches and the power consumption of the switch control circuit. Since the IIC is supplied exclusively by the storage capacitor, any losses within the control circuit are considered. The average power dissipation of the switch control circuit is 4.7 µW.

Fig. 3 shows the transient behavior of \( V_{\text{Rec}} \) over one half period. The peaks are detected properly independently of the absolute value. Due to \( R_{P} \) being not infinitely high, there are two peaks and thus two transfer processes per half period. Fig. 5 shows the detailed behavior of \( V_{\text{Rec}} \), \( IL \) and the switch control waveforms during the transfer processes. The PG current amplitude \( I_{P} = 0.27 \text{ mA} \) has been chosen such that the first and the second transfer process occurs using ST23 and ST13, respectively.

The curves demonstrate that the switchover between the two switching techniques works well. The efficiency of the IIC, \( \eta \), is calculated as follows:

\[
\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{E_{\text{out}}}{E_{\text{in}}} = \frac{E_{\text{out}}}{E_{\text{in}}}, \quad \text{whereas}
\]

\[
E_{\text{out}} = V_{\text{Stor}} \int_{0}^{\text{2}\pi} I_{\text{Stor}} \text{ at and}
\]

\[
E_{m} = 0.5 C_{r} \left( V_{\text{Rec}0/2}^{2} + V_{\text{Rec}0/2}^{2} \right)
\]

**CONCLUSION AND FUTURE ASPECTS**

An efficient self-powered CMOS integrated interface circuit (IIC) for piezoelectric generators (PGs) has been presented. By using high voltage MOSFETs, PG voltage amplitudes up to 18 V can be processed. By the implementation of an improved switching technique, the efficiency could be increased by about 8 % compared to the state-of-the-art switching technique to values between 80 % and 90 % over a large range of PG amplitudes.

The IIC is being layouted and will be fabricated in a chip foundry soon. Measurements with real piezoelectric generators will be made in order to verify the simulation results.

**REFERENCES**